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Fpga Implementation of Rounded Based Approximate Multiplier for Efficient Performance of Digital Signal Processing

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***Abstract*:** *In Recent Technology, Multiplier Plays A Significant Role Of Arithmetic Operations In DSP Applications. A Recent Development In Processor Also Follows The Significant Design Criteria Are High Speed And Power Consumption. Many Current DSP Applications Are Targeted At Portable, Battery-Operated Systems, So That Power Dissipation Becomes One Of The Primary Designs Constrains. Since Multipliers Are Rather Complex Circuits And Typically Operate At A High System Clock Rate. In These Paper, Here Proposing Both Signed And Unsigned Multiplications In Rounded Based Approximate Multiplier. The Digital Reconfiguration Of Finite Impulse Response Architecture Is Inherently Support Multiplier Constant Multiplication (MCM) Technique. So Here Proposed To Design Low Power FIR Filter Using MCM Technique In ROBA Multiplier. This Rounded Based Approximate Multiplier Has High Speed Energy Efficient Process. In Previous Work, Rounded Based Approximate Multipliers Are Not Implemented By Low Power FIR Filter. So Here Proposed To Implement ROBA With FIR Filter For High Accuracy And Power Consumption In FPGA Processor. Finally, The Proposed Architecture Will Designed In VHDL And Synthesized In XILINX FPGA S6LX9, And Shown The Comparison Of Area, Power And Delay.*

***Keywords*-** *FIR Filter, MCM Technique, ROBA Multiplier, Signed Operations, Unsigned Operations.*

I. Introduction

The Minimization Of Energy Is The Main Requirement Of Electronic System, Where It Is Mainly Desired To Achieve High Performance Of Efficient Speed In All Processor. The Requirement Of Every Processor Has High Speed Energy Efficient. To Increase The Speed Of The Processor, Different Multipliers Are Analyzed To Implement The FPGA Processor. The Arithmetic Logic Unit Is The Main Computational Core Blocks Of The DSP Systems. Many Of The DSP Cores Had Implemented In Image And Video Processing. In Addition To The Image And Video Processing Applications Have Other Areas As Arithmetic Operations, Where The Use Of Approximate Multiplier Mainly Desired To Achieve The High Accuracy And Power Consumption. The Adders And Multipliers Are Building Blocks Of The Arithmetic Unit. In This Paper, Proposing A High Speed, Low Power Approximate Multiplier Called ROBA Multiplier. This Means Approximate Multiplier That Has Rounded Value. Therefore, Improving The Speed, Power, And

ENergy Efficient. The Characteristics Of This Multiplier Play A Vital Role In FPGA Processors. A Multiplier Is One Of The Key Bocks In Digital Signal Processing. It Is Typically Operated At High System Clock Rate, And Reducing Delay. The Simplest Way To Perform A Multiplication Is Usage Of Single Two Input Adders. Then Efficiency Of These Structures Is Comparing The Delay, Power, And Energy Consumptions. To Increase The Speed Of The Processor, Different Multipliers Are Analyzed To Implement The FPGA Processor. Here, ROBA Multiplier Is Implemented, Which Means Approximate Multiplier That Has Rounded Value. Therefore, Improving The Speed, Power, And Energy Efficiency. The Characteristics Of Multipliers Are Plays An Vital Role In Every Processors.

The Rest Of This Paper Is Followed As. Section II Discuss About The Previous Work Of Approximate Multipliers. The Proposed Scheme Follows In Section III. ROBA Multiplier With FIR Filter With Its Hardware Work In Section IV. Accuracy Results Are Shown In Section V. In Section VI, Final Conclusion Was Drawn.

II. Prior Work

ROBA-Rounded Based Approximate Multiplier, Which Is Used To Determine The Accuracy Of The Multiplications In FPGA Processor. In Existing Comparison Separate Multiplier Design Is Used For Signed And Unsigned Operations. And It Require More Logic Size And It Consume More Power.

2.1 Signed Operation:

The Signed 2's Complement Operation Is Used To Represent The Negative Operands As Well As Positive Operands In These Multiplications. When This Multiplier Is Negative Represented In Signed 2's Complement. Each 1 Is Added, When It Requires The Addition Of The Multiplicand To The Partial Product.

2.2 Unsigned Operation:

The Positive Number Does Not Require An Arithmetic Sign. An M-Bit Unsigned Number Represent All Numbers Range From 0-255.

2.3 Existing Implementation Of ROBA Multiplier:

The ROBA Multiplier Is Modified By Conventional Multiplication Approach By Assuming The Rounded Values. Three Optimized Structure Was Followed For Both Signed And Unsigned Operations. Where The Inputs Was Represented In Two's Complement Format. When The Sign Of The Inputs Was Determined, And Absolute Value Is Generated For Each Negative Value. Then Rounding Operation Was Made, Where Nearest Approximate Value Was Generated In The Form Of 2n, These Rounded Values Was Represented As Input A And B, Respectively. Then Shifting Operations Was Made. Shifter Register Can Have Both Parallel And Serial Inputs And Outputs .It Is Bidirectional Register Which Allow Shifting In Both Directions, (Left To Right Or Right To Left). Shift Register Are Used To Handle Data Processing.

$A \times B = (Ar - A) \times (Br - B) + Ar \times B + Br \times A - Ar \times Br.$ (1)

$A \times B \sim= Ar \times B + Br \times A - Ar \times Br.$ (2)

When Two Numbers Are Added To Be Stored In Shift Register. It Converts The Data Between The Serial And Parallel Direction. It Is A Temporary Storage In A Processor. An Adder Is Digital Circuit That Performs Addition Of Numbers, It Is Used To Calculate The Addresses, Increment, And Decrement Operators Using Three Shift And Two Addition /Subtraction Method, The Value Of A And B Are Noted. This Is Equal To The Two Nearest Absolute Values 2p And 2p-1. Depending On The Magnitudes Of These Input Exact Multiplications Was Calculated In This Shifting Process. Finally, Absolute Value Of Both Inputs And Outputs Sign Of Multiplication Result Is Based On The Input Sign Be Determined And Then The Operations Be Performed For Unsigned Numbers.

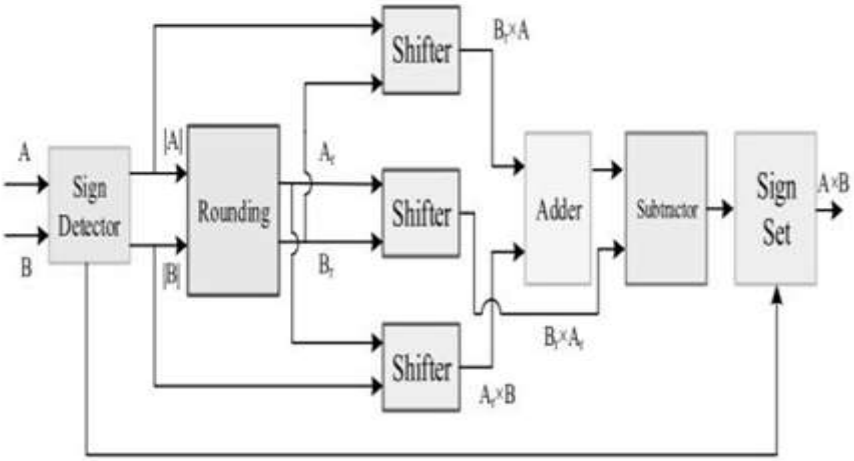

Fig. 1. ROBA Multiplier

III. Proposed System

3.1 Proposed ROBA Multiplier:

ROBA- Rounded Based Approximate Multiplier, Which Is Used To Determine The Approximate Rounded Values. In Previous Work ROBA Is Implemented By Multiple Constant Multiplication Technique (MCM) For Signed And Unsigned Multiplications, Which Is Followed By The Separate MCM Technique. Due To This Separate MCM Technique, There Will Be An Accumulation Of Large Area, Logic Size Was Increased, And Complexity Of Errors Was Obtained. To Overcome This Technique, Here Proposed To Implement The ROBA With FIR Filter. This Means Both Signed And Unsigned Operations In Single ROBA Multiplier. That Increases The Accuracy Of The Multiplications Technique In FPGA Processor. In This Multiplier, MCM Technique Will Propose To Design ROBA With FIR Filter. The Main Drawback Of MCM Technique Will Not Work Both Signed And Unsigned Operations. So To Overcome The Drawback, Here Proposed To Design With Rounded Based Approximate Multiplier.

3.2 FIR Filter

A High Quality Will Generally Has More Multiplications. The FIR Filter Has More Coefficients And Uncommon Adders With Multiplications Are Combined With An Adder. Filtering Coefficient Is Used To Reduce The Complexity Of The Multiplications. FIR Filter Is Widely Used In Several Digital Signals Processing. It Support High Sampling Rate. Each Filter Output Requires Both Addition And Multiplications. Filter Coefficient Are Used To Reduce The Complexity Of Realization Of Multiplications.

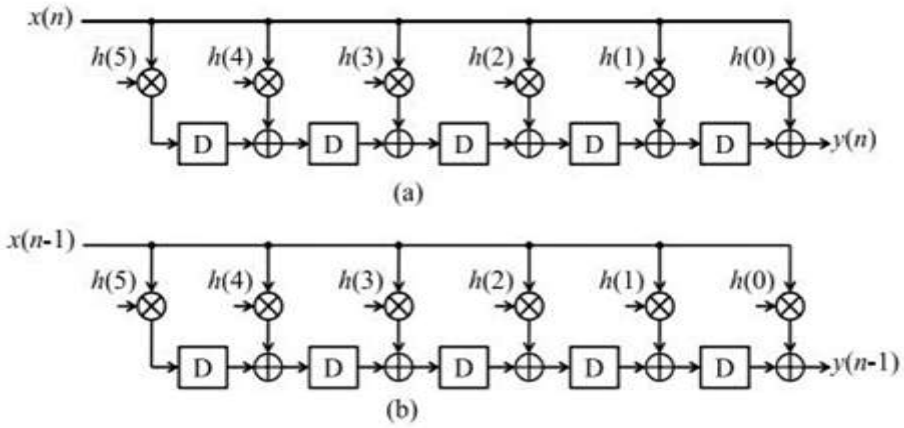

Fig. 2. FIR Filter

3.3 MCM Technique:

The MCM Technique Is Suitable For Implementation Of Large Order FIR Filter. Where MCM Technique Is Followed By Transpose Form Of FIR Filter. These Transpose Form Of Structure Has High Sampling Rate By Using Various Multipliers And Addition. For Each FIR Filter, It Increases The Linearity Function. MCM Technique Improves The Area-Delay Efficiency. In Existing Comparison, Separate Multiplier Design Is Used For Signed And Unsigned Operations In MCM Technique. And It Requires More Logic Size And It Consume Power. The Drawbacks Of MCM Technique Will Not Work Both Thing Of Signed And Un Signed Multiplication. So It Is Need To Design MCM With Rounded Based Approximate Multiplier That Includes Both Signed And Unsigned Operation In Single Multiplier.

3.4 Proposed Approximate Multiplier With FIR Filter:

FIR Filter Is Widely Used For Several Digital Signal Processing. The Frequency Specifications Require The Large Order FIR Filter. These Filter Support High Sampling Rate For High-Speed Digital Communications. A Real Time Implementation Of Large Order FIR Filter Increases The Linearity Function. Several Design For Efficient Realizations Of FIR

Filters Uses The Multiple Constant Multiplication Methods. This MCM Technique Reduces The Different Complexity. The Realizations Of Multiplications Give The Input, Which Is Multiplied With Set Of Constants. This MCM Approach Mainly Implemented By Large Order FIR Filter. It Improves The Area-Delay Efficiency. Due To The High Sampling Rate, It Operates On Transpose Form Of Structure. The Filtering Coefficients Are Utilized To Reduce The Complexity Of The Realization Of Multiplications.

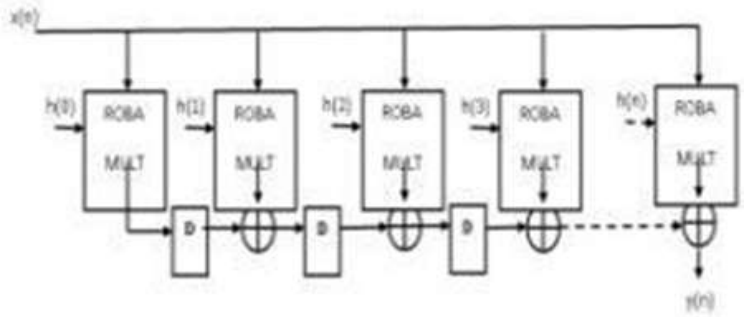

Fig. 3. ROBA Multiplier With FIR Filter

Energy Efficiency Is The Main Requirements Of Electronics System. The Computational Core Of These Blocks Has Arithmetic Logic Unit Where Multiplications Have Greatest Performance In DSP Systems. It Can Perform The Multiplication Operation Using Three Shift And Two Addition And Subtraction Operations. The Main Advantages Of The Proposed ROBA Multiplier Exist Only For Positive Inputs. Because It Is Followed By Two's Complement Representation. Where The Values Of Negative Inputs Are Not In The Form Of 2n.The Absolute Value Of The Both Input And Output Is Based On The Determination Of Input Signs. In These Multiplier, Conventional Multiplication Approach Is Modified By New Scheme Of ROBA Multiplication. First The Sign Of The Inputs Are Mentioned, Where Inputs Are Represented In Two's Complement Format, And For Each Negative Value, The Absolute Value Is Generated.
Here The Following Equation To Determine Each Output Bit Of The Rounding Block In ROBA Multiplier.

3.5 Proposed Adder Design:

3.5.1 HMPE Structure:

The HMPE Structure Consists Of Two Parts,
A Regular Prefix Adder
A Modified Excess-One Unit

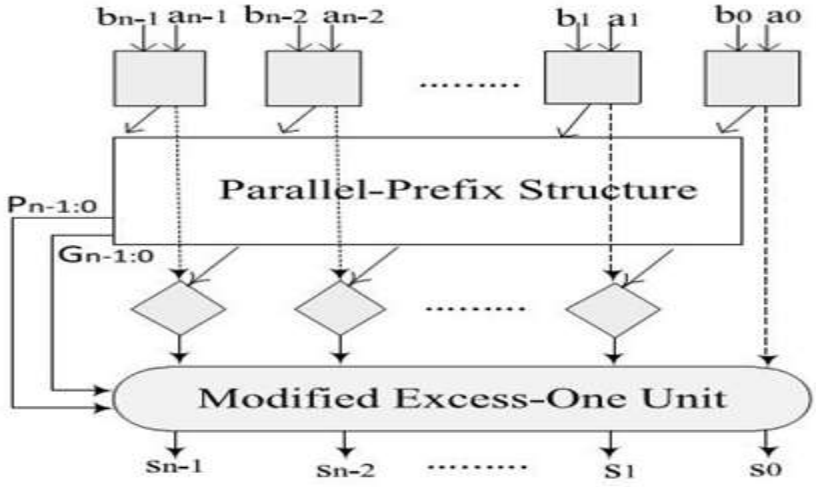

Fig. 4. HMPE Structure

First, The Two Operands Are Added Using Prefix And The Result Is Conditionally Incremented Based On Control Signals Generated By The Prefix Structure.

3.5.2 Parallel Prefix Structure:

The Parallel-Prefix Structure Is Found To Be In High Performance Adders Because Of The Delay Is Logarithmically Proportional To The Adder.

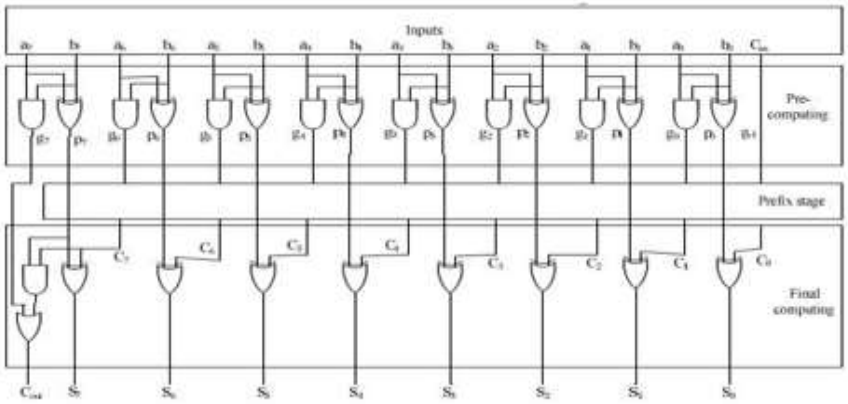

Fig. 5. Parallel Prefix Adder

It Consist Of 3stages

3.5.2.1 Pre Computation:

In Pre Computation Stage, Here Two Inputs Are Generated And Computed.

Pi = Ai XOR Bi

Gi = Ai AND Bi

3.5.2.2 Prefix Stage:

In The Prefix Stage, Generation And Computation Of The Signal Are Computed At Each Bit. The Black Cell Generates The Ordered Pair In The Gray Cell, Where It Generates Only The Left Signal.

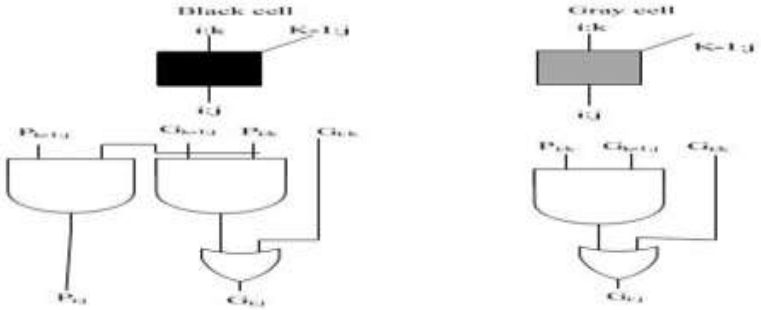

Fig. 6. Prefix Stage

3.5.2.3 Final Computation:

In The Final Computation, The Sum And Carry Are The Final Output. Where "-1" Represent The Position Of The Carry Input Values. Based On The Different Ways Of Grouping, Different Prefix Architecture Are Created.

Si =Pi And Gi-1:-1
C Out = G N:-1

IV. Analysis Of Experimental Results

Here, The Implementation Of Rounded Based Approximate Multiplier With FIR Filter Shown The Results Of Area, Power And Timing Report.

3.5.3 16 Bit Brent Kung Adder:

Brent Kung Adder Is A Very Well-Known Logarithmic Adders. It Has Different Intermediate Nodes. The Main Drawback Of This Adder Is, Thus The Rise Time And Fall Time Nodes Does Not Same. So, To Overcome This Drawback Buffer Stages Are Used With The Precomputation Process. Where It Generate The Inputs And Propagate The Outputs From This Adders

V. Hardware Implementation

The Input Will Provided Through UART Interface Communication Regarding The Input Frequency, It Undergoes For Testing. The Designing Of Low Pass Filter With ROBA Multiplier At Sampling Frequency (Fs) =5MHZ. So, Here Need To Test The Input Frequency Range Up To 1-10 MHZ, Where The NCO/VCO Will Help For Frequency Range Up To 1-10 MHZ, The Input Frequency Will Provided To FIR Filter With ROBA Multiplier, And The Output Frequency Will Provided Through DAC, And Test The DAC Output Using Oscilloscope. The Main Advantages Are Followed As Common Multiplier Design For Signed And Unsigned Operations, And Less Logic Size, Power, And Delay.

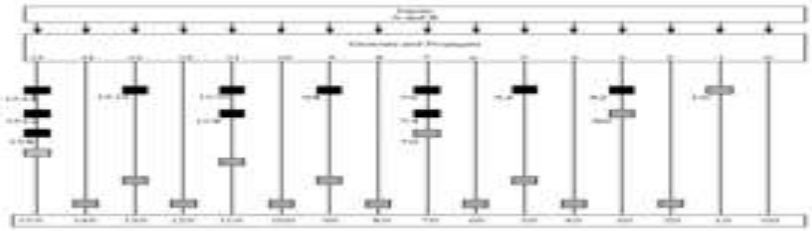

Fig. 7. 16 Bit Brent Kung Adder

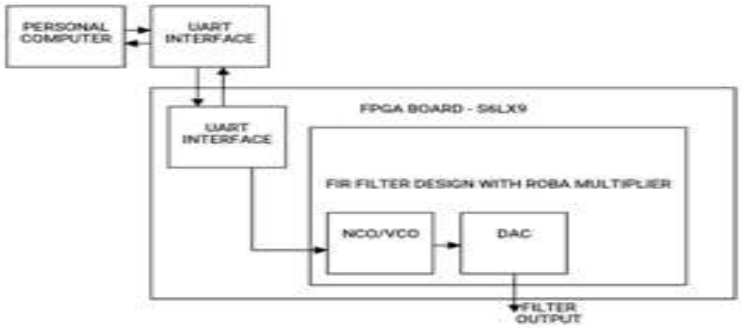

Fig. 8. Hardware implementation of ROBA with FIR filter

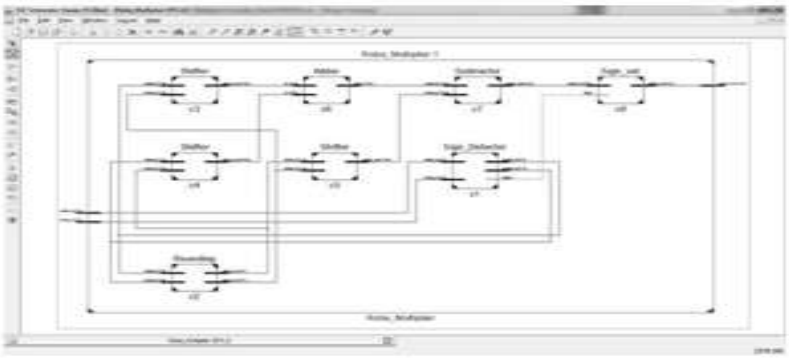

Fig. 9. RTL View Of ROBA Multiplier

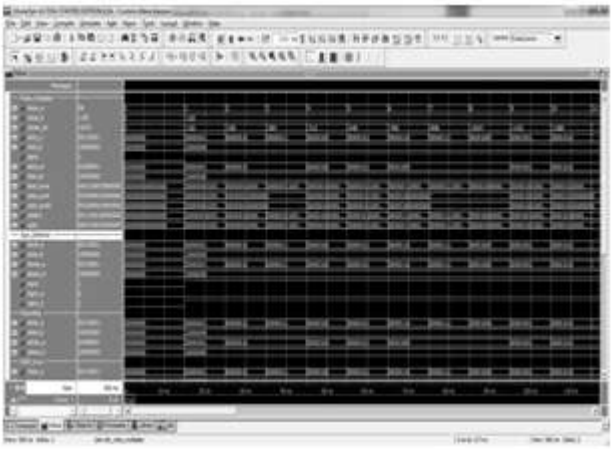

Fig. 10. Simulation Results Of ROBA 1

Fig. 11. Simulation Results Of ROBA With FIR Filter 1

Fig. 12. Simulation Results Of ROBA With FIR Filter 2

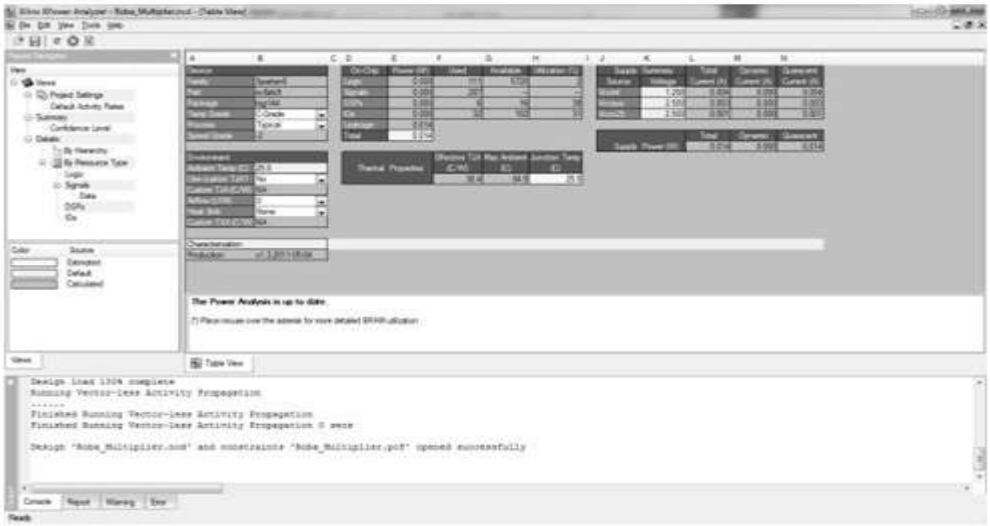

Fig. 13. Power Report

TABLE 1. COMPARISON FOR EXISTING AND PROPOSED SYSTEM

Contents	Existing System - 8TAP	Proposed System-16TAP
Number of Slice Registers	-	751
Number of Slice LUT	1508	2005
Number of Occupied Slice	-	721
Number of IOB	-	26
Total Power (mW)	85	14
Dynamic Power (nW)	-	1
Delay(ns)	1.280	17.980
Fanout effect	-	2.42

Fig. 14. Graphical Representation Of Power Report

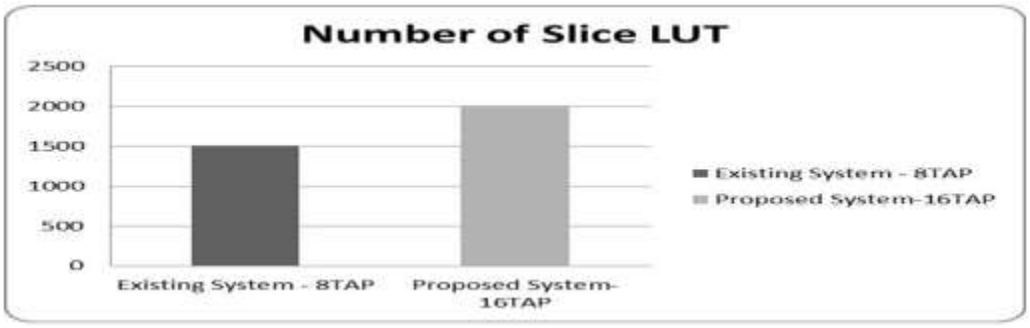

Fig. 15. Graphical Representation Of Area Analysis

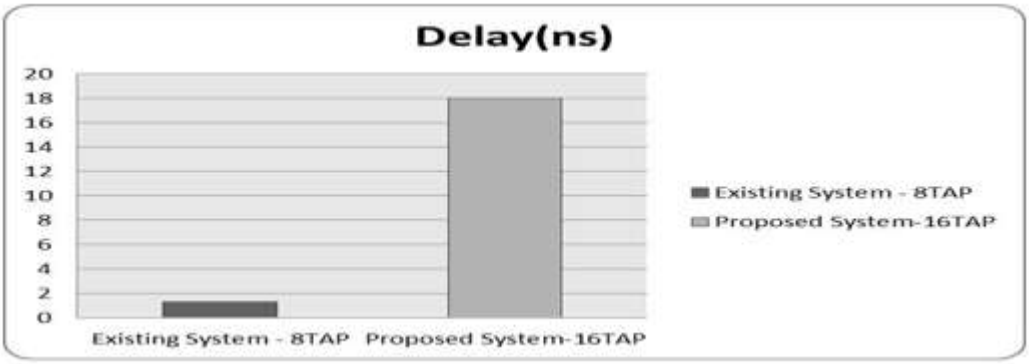

Fig. 16. Analysis Of Delay Report Graphical

Finally, It Can Be Seen That The Implementation Of Rounded Based Approximate Multiplier With FIR Filter Shown The Frequency Coefficient Of FIR Filter.
Usage Of Power Report = 14mw
Delay Report = 17.980ns

VI. Conclusion

The Proposed Multiplier Is Used To Improve The Speed And Energy Consumption. It Is Used In Digital Signal Processing, By Proposing An ROBA Multiplier, It Has High Accuracy. Considering In The Future, Low Power VLSI Design Need Number Of Bits. It May Increase The Encoding Scheme . The Power Can Be Reduced By Improving The Partial Product Compression Ratio.

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